Nets. Models can be given in several instances parameterized by scaling parameters. Colored nets can be accompanied by one or many equivalent, unfolded $P / T$ nets. Models are given together with property files (possibly, one per model instance) giving a set of properties to be checked on the model.

## Description

This model describes a hardware circuit component designed at Tiempo Secure ${ }^{(a)}$, namely, an on-chip asynchronous serial link, the architecture of which is illustrated in the Figure below. This link enables the interconnection of a set of IP ${ }^{(\mathrm{b})}$ slaves designed by other vendors. Each IP slave is synchronous, must be reused as such, and can be accessed through a standard interface such as ARM's AMBA-APB ${ }^{(c)}$.
The asynchronous serial link establishes a bridge between, on the one hand, the set of IP slaves, which are daisy-chained, and, on the other hand, a synchronous master IP. It is easily configurable to fit any number of IP slaves and locations. A key feature of the link is its design based on asynchronous logics [1][2], which brings physical and logical reliability (due to the delay-insensitive implementation) and easy integration in $\mathrm{SoCs}^{(\mathrm{d})}$ with multiple power and clock domains (because of the variability tolerance, the absence of clock, and the low wire count of the asynchronous implementation).

Following the modelling and verification methodology [3] adopted at Tiempo Secure, the asynchronous serial link was formally specified using the LNT language supported by the verification tools available in the CADP toolbox. The considered LNT specification covers the architectural part delimited by the dashed line in the Figure below. A scalable family of ten LNT specifications was made by increasing from one to ten the number of IP slaves connected to the asynchronous link.

Each LNT specification was translated automatically to LOTOS, and then to an interpreted Petri net using the CADP toolbox. Finally, a P/T net was obtained by stripping out all data-related information (variables, types, assignments, guards, etc.) from the interpreted Petri net, leading to a NUPN (Nested-Unit Petri Net) model translated to PNML using the CÆSAR.BDD tool.
Each instance of the model is parameterized by the number $N$ of IP slaves, and also by its version $V$, which specifies how the NUPN has been produced from the LOTOS specification. $V$ is either equal to " $a$ " if the NUPN has been generated after applying all the structural and data-flow optimizations of the CÆSAR compiler for LOTOS, or to " $b$ " if the NUPN has been generated before these optimizations.


Architecture of the Asynchronous Serial Link

[^0]Model: ASLink Type: P/T Net Aymane Bouzafour, Marc Renaudin, and Hubert Garavel Origin: Industrial since

## References

[1] Marc Renaudin. Asynchronous Circuits and Systems: A Promising Design Alternative. In Microelectronics for Telecommunications: Managing High Complexity and Mobility (MIGAS'2000), special issue of the Microelectronics Engineering Journal, vol. 54, num. 1-2, Elsevier, Dec. 2000.
[2] Jens Sparsø. Asynchronous Circuit Design: A Tutorial. Technical University of Denmark, March 2006. Available from http://www.imm.dtu.dk/~jsp.
[3] Aymane Bouzafour, Marc Renaudin, Hubert Garavel, Radu Mateescu, and Wendelin Serwe. Model-checking Synthesizable SystemVerilog Descriptions of Asynchronous Circuits. In Proceedings of the 24th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC'18), Vienna, Austria, May 2018.

## Scaling parameter

| Parameter name | Parameter description | Chosen parameter values |
| :--- | :--- | :--- |
| $N$ | $N$ is the number of IP slaves | from 1 to 10 |

## Size of the model

| Parameter | Number of <br> places | Number of <br> transitions | Number of <br> arcs | Number of <br> units | HWB code |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $N=01, V=a$ | 431 | 735 | 2801 | 83 | $4-75-196$ |
| $N=01, V=b$ | 846 | 1148 | 3624 | 105 | $12-75-284$ |
| $N=02, V=a$ | 626 | 1008 | 3820 | 118 | $4-104-281$ |
| $N=02, V=b$ | 1242 | 1621 | 5041 | 153 | $13-104-409$ |
| $N=03, V=a$ | 821 | 1281 | 4839 | 153 | $4-133-366$ |
| $N=03, V=b$ | 1638 | 2094 | 6458 | 201 | $14-133-534$ |
| $N=04, V=a$ | 1016 | 1554 | 5858 | 188 | $4-162-451$ |
| $N=04, V=b$ | 2034 | 2567 | 7875 | 249 | $15-162-659$ |
| $N=05, V=a$ | 1211 | 1827 | 6877 | 223 | $4-191-536$ |
| $N=05, V=b$ | 2430 | 3040 | 9292 | 297 | $16-191-784$ |
| $N=06, V=a$ | 1406 | 2100 | 7896 | 258 | $4-220-621$ |
| $N=06, V=b$ | 2826 | 3513 | 10709 | 345 | $17-220-909$ |
| $N=07, V=a$ | 1601 | 2373 | 8915 | 293 | $4-249-706$ |
| $N=07, V=b$ | 3222 | 3986 | 12126 | 393 | $18-249-1034$ |
| $N=08, V=a$ | 1796 | 2646 | 9934 | 328 | $4-278-791$ |
| $N=08, V=b$ | 3618 | 4459 | 13543 | 441 | $19-278-1159$ |
| $N=09, V=a$ | 1991 | 2919 | 10953 | 363 | $4-307-876$ |
| $N=09, V=b$ | 4014 | 4932 | 14960 | 489 | $20-307-1284$ |
| $N=10, V=a$ | 2186 | 3192 | 11972 | 398 | $4-336-961$ |
| $N=10, V=b$ | 4410 | 5405 | 16377 | 537 | $21-336-1409$ |

## Structural properties

ordinary - all arcs have multiplicity one simple free choice - all transitions sharing a common input place have no other input place
 state machine - every transition has exactly one input place and exactly one output place ....................... $\boldsymbol{X}$
marked graph - every place has exactly one input transition and exactly one output transition
connected - there is an undirected path between every two nodes (places or transitions)

[^1]strongly connected - there is a directed path between every two nodes (places or transitions)
 sink place(s) - one or more places have no output transitions
source transition(s) - one or more transitions have no input places
sink transitions(s) - one or more transitions have no output places
loop-free - no transition has an input place that is also an output place
conservative - for each transition, the number of input arcs equals the number of output arcs (o)
subconservative - for each transition, the number of input arcs equals or exceeds the number of output arcs $\boldsymbol{X}(\mathrm{p})$ $\boldsymbol{X}$ (q) nested units - places are structured into hierarchically nested sequential units ${ }^{(\mathrm{r})}$

## Behavioural properties

 dead place(s) - one or more places have no token in any reachable marking .................................................? dead transition(s) - one or more transitions cannot fire from any reachable marking ........................................? deadlock - there exists a reachable marking from which no transition can be fired ..........................................? reversible - from every reachable marking, there is a transition path going back to the initial marking ...................? live - for every transition $t$, from every reachable marking, one can reach a marking in which $t$ can fire $\qquad$

## Size of the marking graphs

| Parameter | Number of reachable markings | Number of transition firings | Max. number of tokens per place | Max. number of tokens per marking |
| :---: | :---: | :---: | :---: | :---: |
| $N=01, V=a$ | $\geq 8.74114 \mathrm{e}+07^{(\mathrm{t})}$ | ? | $1{ }^{\text {(u) }}$ | $\in[21,75]^{(\mathrm{v})}$ |
| $N=01, V=b$ | $\geq 2.09328 \mathrm{e}+11^{(\mathrm{w})}$ | ? | $1^{(\mathrm{x})}$ | $\in[19,75]^{(y)}$ |
| $N=02, V=a$ | $\geq 1.0807 \mathrm{e}+09^{(\mathrm{z})}$ | ? | $1{ }^{\text {(aa) }}$ | $\in[31,104]^{\text {(ab) }}$ |
| $N=02, V=b$ | $\geq 5.69187 \mathrm{e}+14^{\text {(ac) }}$ | ? | $1^{\text {(ad) }}$ | $\in[29,104]^{\text {(ae) }}$ |
| $N=03, V=a$ | $\geq 7.51327 \mathrm{e}+10^{\text {(af) }}$ | ? | $1{ }^{\text {(ag) }}$ | $\in[41,133]^{\text {(ah) }}$ |
| $N=03, V=b$ | $\geq 1.24479 \mathrm{e}+22^{\left({ }^{\text {ai) }}\right.}$ | ? | $1^{\text {(aj) }}$ | $\in[39,133]^{\text {(ak) }}$ |
| $N=04, V=a$ | $\geq 6.9673 \mathrm{e}+06^{\text {(al) }}$ | ? | $1^{(a m)}$ | $\in[51,162]^{\text {(an) }}$ |
| $N=04, V=b$ | $\geq 4.86333 \mathrm{e}+27^{\text {(ao) }}$ | ? | $1{ }^{\text {(ap) }}$ | $\in[49,162]^{\text {(aq) }}$ |
| $N=05, V=a$ | $\geq 1.67215 \mathrm{e}+08^{\text {(ar) }}$ | ? | $1^{\text {(as) }}$ | $\in[61,191]^{\text {(at) }}$ |
| $N=05, V=b$ | $\geq 1.27462 \mathrm{e}+33^{(\mathrm{au})}$ | ? | $1^{\text {(av) }}$ | $\in[59,191]^{\text {(aw) }}$ |
| $N=06, V=a$ | $\geq 2.08612 \mathrm{e}+20^{(\mathrm{ax})}$ | ? | $1^{\text {(ay) }}$ | $\in[71,220]^{(\mathrm{az})}$ |
| $N=06, V=b$ | $\geq 3.43882 \mathrm{e}+38^{\text {(ba) }}$ | ? | $1{ }^{\text {(bb) }}$ | $\in[69,220]^{\text {(bc) }}$ |
| $N=07, V=a$ | $\geq 2.00858 \mathrm{e}+23^{\text {(bd) }}$ | ? | $1{ }^{\text {(be) }}$ | $\in[81,249]^{\text {(bf) }}$ |
| $N=07, V=b$ | $\geq 2.06918 \mathrm{e}+44^{(\mathrm{bg})}$ | ? | $1{ }^{\text {(bh) }}$ | $\in[79,249]^{\text {(bi) }}$ |
| $N=08, V=a$ | $\geq 1.25256 \mathrm{e}+26^{(\mathrm{bj})}$ | ? | $1^{\text {(bk) }}$ | $\in[91,278]^{\text {(bl) }}$ |
| $N=08, V=b$ | $\geq 1.3975 \mathrm{e}+49$ (bm) | ? | $1^{\text {(bn) }}$ | $\in[89,278]^{\text {(bo) }}$ |
| $N=09, V=a$ | $\geq 1.18847 \mathrm{e}+29{ }^{(\mathrm{bp})}$ | ? | $1^{\text {(bq) }}$ | $\in[101,307]^{\text {(br) }}$ |
| $N=09, V=b$ | $\geq 6.32435 \mathrm{e}+54^{\text {(bs) }}$ | ? | $1{ }^{\text {(bt) }}$ | $\in[99,307]^{\text {(bu) }}$ |
| $N=10, V=a$ | $\geq 6.65672 \mathrm{e}+31^{(\mathrm{bv})}$ | ? | $1^{\text {(bw) }}$ | $\in[111,336]^{(\mathrm{bx})}$ |
| $N=10, V=b$ | $\geq 1.7836 \mathrm{e}+58^{\text {(by) }}$ | ? | $1^{\text {(bz) }}$ | $\in[109,336]^{\text {(ca) }}$ |

[^2][^3][^4]
[^0]:    (a) http://www.tiempo-secure.com
    ${ }^{(b)}$ see http://en.wikipedia.org/wiki/Semiconductor_intellectual_property_core
    ${ }^{(c)}$ see http://en.wikipedia.org/wiki/Advanced_Microcontroller_Bus_Architecture
    ${ }^{(d)}$ see http://en.wikipedia.org/wiki/System_on_a_chip

[^1]:    ${ }^{(e)}$ stated by CÆSAR.BDD version 2.7 on all 20 instances ( 10 values of $N$ ).
    ${ }^{(f)}$ stated by CÆSAR.BDD version 2.7 on all 20 instances ( 10 values of $N$ ).
    ${ }^{(\mathrm{g})}$ stated by CÆSAR.BDD version 2.7 on all 20 instances $(10$ values of $N)$.
    ${ }^{(h)}$ stated by CÆSAR.BDD version 2.7 on all 20 instances ( 10 values of $N$ ).
    ${ }^{(i)}$ stated by CÆSAR.BDD version 2.7 on all 20 instances ( 10 values of $N$ ).

[^2]:    (j) from place 1 one cannot reach place 0 .
    ${ }^{(\mathrm{k})}$ place 0 is a source place.
    ${ }^{(1)}$ stated by CÆSAR.BDD version 2.7 on all 20 instances ( 10 values of $N$ ).
    ${ }^{(\mathrm{m})}$ stated by CÆSAR.BDD version 2.7 on all 20 instances $(10$ values of $N)$.
    ${ }^{(\mathrm{n})}$ stated by CÆSAR.BDD version 2.7 on all 20 instances ( 10 values of $N$ ).
    ${ }^{(o)}$ stated by CÆSAR.BDD version 2.7 on all 20 instances ( 10 values of $N$ ).
    (p) stated by CÆSAR.BDD version 2.7 on all 20 instances ( 10 values of $N$ ).
    (q) stated by CÆSAR.BDD version 2.7 on all 20 instances ( 10 values of $N$ ).
    ${ }^{(r)}$ the definition of Nested-Unit Petri Nets (NUPN) is available from http://mcc.lip6.fr/nupn.php
    ${ }^{(s)}$ safe by construction - stated by the CÆSAR compiler.
    ${ }^{(t)}$ stated by CÆSAR.BDD version 2.7.

[^3]:    (u) stated by the CÆSAR compiler.
    (v) upper bound given by the number of leaf units.
    ${ }^{(\mathrm{w})}$ stated by CÆSAR.BDD version 2.7.
    (x) stated by the CÆSAR compiler.
    (y) upper bound given by the number of leaf units.
    ${ }^{(\mathrm{z})}$ stated by CÆSAR.BDD version 2.7.
    (aa) stated by the CÆSAR compiler.
    (ab) upper bound given by the number of leaf units.
    (ac) stated by CÆSAR.BDD version 2.7.
    (ad) stated by the CÆSAR compiler.
    (ae) upper bound given by the number of leaf units.
    (af) stated by CÆSAR.BDD version 2.7 .
    (ag) stated by the CÆSAR compiler.
    (ah) upper bound given by the number of leaf units.
    ${ }^{(a i)}$ stated by CÆSAR.BDD version 2.7 .
    (aj) stated by the CÆSAR compiler.
    (ak) upper bound given by the number of leaf units.
    (al) stated by CÆSAR.BDD version 2.7.
    (am) stated by the CÆSAR compiler.
    (an) upper bound given by the number of leaf units.
    (ao) stated by CÆSAR.BDD version 2.7.
    (ap) stated by the CÆSAR compiler.
    (aq) upper bound given by the number of leaf units.
    (ar) stated by CÆSAR.BDD version 2.7.
    (as) stated by the CÆSAR compiler.
    (at) upper bound given by the number of leaf units.
    (au) stated by CÆSAR.BDD version 2.7.
    (av) stated by the CÆSAR compiler.
    (aw) upper bound given by the number of leaf units.
    (ax) stated by CÆSAR.BDD version 2.7 .
    (ay) stated by the CÆSAR compiler.
    (az) upper bound given by the number of leaf units.
    (ba) stated by CÆSAR.BDD version 2.7.
    (bb) stated by the CÆSAR compiler.
    (bc) upper bound given by the number of leaf units.
    (bd) stated by CÆSAR.BDD version 2.7.
    (be) stated by the CÆSAR compiler.
    (bf) upper bound given by the number of leaf units.
    (bg) stated by CÆSAR.BDD version 3.3.
    (bh) stated by the CÆSAR compiler.
    (bi) upper bound given by the number of leaf units.
    (bj) stated by CÆSAR.BDD version 2.7.
    (bk) stated by the CÆSAR compiler.
    (bl) upper bound given by the number of leaf units.
    (bm) stated by CÆSAR.BDD version 3.3.
    (bn) stated by the CÆSAR compiler.
    (bo) upper bound given by the number of leaf units.
    (bp) stated by CÆSAR.BDD version 2.7.
    (bq) stated by the CÆSAR compiler.
    (br) upper bound given by the number of leaf units.
    (bs) stated by CÆSAR.BDD version 3.3.
    (bt) stated by the CÆSAR compiler.
    (bu) upper bound given by the number of leaf units.
    (bv) stated by CÆSAR.BDD version 3.3.
    (bw) stated by the CÆSAR compiler.
    (bx) upper bound given by the number of leaf units.
    (by) stated by CÆSAR.BDD version 3.3.

[^4]:    (bz) stated by the CÆSAR compiler.
    (ca) upper bound given by the number of leaf units.

